REMARKS

Favorable reconsideration of this application, as presently amended and in light of the following discussion, is respectfully requested.

Claims 9-14 and 16-24 are currently pending. Claims 9, 10, 16, and 21 have been amended; Claims 1-8 and 15 have been canceled; and Claims 22-24 have been added by the present amendment. The changes and additions to the claims are supported by the originally filed specification and do not add new matter.

In the outstanding Office Action, Claims 1, 2, 16, and 21 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Application Publication No. U.S. 2004/0199841 to Marr (hereinafter "the '841 application"); Claims 17 and 18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the '841 application in view of "Applicant's admitted prior art" (hereinafter "the Background Art"); and Claims 3-15, 19, and 20 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form.

Applicant respectfully submits that the rejections of Claims 1 and 2 under 35 U.S.C. § 102 are rendered moot by the present cancellation of those claims. However, Applicant notes that new Claim 22 includes the limitations of canceled Claims 1 and 2.

New Claim 22 is directed to a semiconductor apparatus having a logic level decision circuit, the logic level decision circuit comprising: (1) a first comparison circuit which compares an input signal with a first reference signal corresponding to logic "1" level, and which outputs a first differential signal; (2) a second comparison circuit which compares the input signal with a second reference signal corresponding to logic "0" level, and which outputs a second differential signal; and (3) a third comparison signal which compares the output of the first comparison signal and the output of the second comparison circuit, and which decides a logic level of the input signal. Further, new Claim 22 recites that the logic

level decision circuit is an input receiver which decides the logic level of an external input signal, and that the first and second reference signals are inputted from outside of the semiconductor apparatus. New Claim 22 is supported by the originally filed specification and does not add new matter.¹

Applicant respectfully submits that new Claim 22 patentably defines over the '841 application.

The '841 application is directed to a midpoint detection circuit 200 that generates a midpoint signal MS by detecting the midpoint of an input signal SIN in order to enter a test mode. As shown in Figure 3, the '841 application shows another embodiment of the midpoint detection circuit shown in Figure 2A of the '841 application. As shown in Figure 3, the '841 application discloses that the midpoint detection circuit 200 has reference voltages VREF1 and VREF2 supplied to a pair of differential amplifiers 222 and 224, respectively. However, Applicant respectfully submits that the '841 application fails to disclose first and second reference signals that are inputted from outside of the semiconductor apparatus, as recited in new Claim 22. Rather, the reference voltages VREF1 and VREF2 disclosed by the '841 application are generated inside the chip. Accordingly, Applicant respectfully submits that new Claim 22 patentably defines over the '841 application.

New Claims 16 and 21 recite limitations analogous to the limitations recited in new Claim 22. Accordingly, for the reasons stated above for the patentability of Claim 22, Applicant respectfully submits that the rejection of Claims 16 and 21 (and all similarly rejected dependent claims) are rendered moot by the present amendment to independent Claims 16 and 21.

Regarding the rejection of dependent Claims 17 and 18 under 35 U.S.C. § 103,

Applicant respectfully submits that the Background Art fails to remedy the deficiencies of the

-

¹ See, e.g., Figure 5 and the discussion related thereto in the specification.

- Application No. 10/623,559

Reply to Office Action of January 30, 2006

'841 application, as discussed above. Accordingly, for the reasons stated above for the

patentability of Claim 16, Applicant respectfully submits that the rejections of Claims 17 and

18 are rendered moot by the present amendment to Claim 16.

The present amendment also sets forth new Claims 23 and 24 for examination on the

merits. New Claim 23 recites the limitations recited in original Claims 1 and 7. Moreover,

new Claim 24 recites the limitations recited in original Claims 1 and 8. Accordingly,

Applicant respectfully submits that new Claims 23 and 24 are supported by the originally

filed specification and do not add new matter. Moreover, based on the indicated allowability

of Claims 7 and 8, Applicant respectfully submits that new Claims 23 and 24 (and all

associated dependent claims) are in condition for formal allowance.

Thus, it is respectfully submitted that independent Claims 16 and 21-24 (and all

associated dependent claims) patentably define over any proper combination of the '841

application and the Background Art.

Consequently, in view of the present amendment and in light of the above discussion,

the outstanding grounds for rejection are believed to have been overcome. The application as

amended herewith is believed to be in condition for formal allowance. An early and

favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,

MAIER & NEUSTADT, P.C.

Customer Number

22850

Tel: (703) 413-3000

Fax: (703) 413 -2220

(OSMMN 03/06)

1:\ATTY\KMB\240's\240522US\240522US-AM.DOC

Eckhard H. Kuesters

Attorney of Record

Registration No. 28,870

Kurt M. Berger, Ph.D.

Registration No. 51,461

12